CLAIMS

1. A multiple-level memory cell, comprising:

a memorization element formed of several polysilicon resistors (Rp1, Rp2, Rp3, Rp4, Rp5, Rp6) associated in series between two input/output terminals (11, 12); and

a load (Rf) in series with said resistive element, the junction point (12) thereof forming a read terminal of the memory cell, and the respective junctions (14, 15, 17, 18, 19) between said resistors of the memorization element being accessible.

2. The cell of claim 1, wherein at least certain points among said junctions (14, 15, 17, 18, 19) of the memorization element and the junction (16) of this element with the load, are connectable, individually by a switch (MN1, MP2, MN3, MP4, MN5, MP6), either to one of said input/output terminals (11, 12) of the memorization element, or to a terminal (13) of application of a predetermined voltage.

3. The cell of claim 2, wherein the ends of a same resistor (Rp1, Rp2, Rp3, Rp4, Rp5, Rp6) are not connectable to the same terminal.

4. The cell of claim 2, wherein said switches comprise MOS transistors distributed half and half between P-channel transistors (MP2, MP4, MP6) and N-channel transistors (MN1, MN3, MN5).

5. The cell of claim 1, wherein all polysilicon resistors (Rp1, Rp2, Rp3, Rp4, Rp5, Rp6) have identical nominal values.

6. The cell of claim 1, wherein the number of possible programmable levels corresponds, at most, to the number of polysilicon resistors (Rp1, Rp2, Rp3, Rp4, Rp5, Rp6) of the memorization element plus one.

7. The memory cell of claim 1, wherein the programming is performed by imposing, in one or several of said polysilicon resistors of the memorization element, a constraint current greater than a current for which the value of this resistance exhibits a maximum.

8. The cell of claim 7, wherein said constraint current is beyond a read operating current range of the memorization element.

9. A circuit for reading from at least one memory cell of claim 1, comprising an assembly of comparators (23, 24; 41, 42, 43) respectively receiving, on a first input, the voltage at the input/output terminals (11, 12) of the memorization elements and, on a second input, a reference voltage (Vref) chosen according to a level to be detected by the comparator from among the desired possible levels.

10. The circuit of claim 9, comprising one comparator less than there are levels desired to be distinguished in the memory cell, and an assembly of logic gates generating as many states as there are comparators, the binary word provided by said assembly representing the state of the memory cell.

11. The circuit of claim 9, comprising a number of comparators equal to twice the number of levels which are desired to be distinguished in the cell, the comparator outputs being combined two by two in the increasing order of the reference voltages that they receive, to detect one level per comparator pair.